AMENDMENTS TO THE CLAIMS:

1. (currently amended): A method for testing for the occurrence of bit errors comprising the steps off:

converting and demultiplexing a ~~testing~~ serial signal for testing purposes into parallel signals corresponding to channels ~~for~~ respectively assigned to a plurality of measured devices and a redundant channel ~~to be demultiplexed for the measured devices~~;

converting a ~~passing~~ signal passing through the redundant channel into a channel determination signal for specifying an alignment of the measured devices;

multiplexing output signals of the measured devices and the channel determination signal corresponding to a demultiplexing mode used for demultiplexing the serial signal; and

measuring occurrence of bit errors ~~from~~ in the multiplexed signals and detecting measured devices ~~concerning~~ at which the bit errors are generated ~~from~~ in consideration of the channel determination signal.

2. (currently amended): The method for testing for the occurrence of bit errors as claimed in claim 1 wherein the channel determination signal comprises a signal in which all bits of the ~~passing~~ signal ~~of~~ passing through the redundant channel are inverted.

3. (currently amended): The method for testing for the occurrence of bit errors as claimed in claim 1 wherein the ~~testing~~ signal for testing purposes has a pseudo random pattern.

4. (currently amended): A device for testing for the occurrence of bit errors comprising:

a signal generator for generating a ~~testing~~ serial signal for testing purposes;

a signal demultiplexer for converting and demultiplexing the serial signal into parallel signals corresponding to channels ~~for~~ respectively assigned to a plurality of measured devices and a redundant channel ~~to be demultiplexed for the measured devices~~;

a channel determination signal generating circuit for converting a ~~passing~~ signal passing through the redundant channel into a channel determination signal for specifying an alignment of the measured devices;

a signal multiplexer for multiplexing output signals of the measured devices and the channel determination signal corresponding to a demultiplexing mode of the signal demultiplexer used for demultiplexing the serial signal; and

a bit error measuring device for measuring occurrence of bit errors ~~from~~ in output signals of the signal multiplexer and detecting measured devices ~~concerning~~ at which the bit errors are generated ~~from~~ in consideration of the channel determination signal.

5. (currently amended): The device for testing for the occurrence of bit errors as claimed in claim 4 wherein the channel determination signal comprises a signal in which all bits of the ~~passing~~ signal ~~of~~ passing through the redundant channel are inverted.

6. (currently amended): The method for testing for the occurrence of bit errors as claimed in claim 2 wherein the ~~testing~~ signal for testing purposes has a pseudo random pattern.